Printed page:03 Subject Code: **BEC0403**

Roll No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B. Tech

SEM: IV- THEORY EXAMINATION (2024-2025)

Subject **CMOS Digital Integrated Circuit**

Time: 3:00 Hours Max. Marks:100

General Instructions:

IMP: Verify that you have received question paper with correct course, code, branch etc.

1. *This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
2. *Maximum marks for each question are indicated on right hand side of each question.*
3. *Illustrate your answers with neat sketches wherever necessary.*
4. *Assume suitable data if necessary.*
5. *Preferably, write the answers in sequential order.*
6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION – A 20

1. Attempt all parts:-

1-a. Which step is typically the first in the VLSI design flow? (CO1,K2) 1

a) Physical design
b) Logic synthesis
c) Specification
d) Floor planning

1-b. In CMOS n-Well process, the n-well is used for placing: (CO1,K2) 1

a) NMOS only
b) PMOS only
c) Both NMOS and PMOS
d) None of the above

1-c. Which of the following defines the noise margin high (NMH)? (CO2,K2) 1

a) VIH - VIL
b) VOH - VIH
c) VIH - VOH
d) VOH - VOL

1-d. What determines the threshold voltage (Vth) of a CMOS inverter? (CO2,K2) 1

a) Only PMOS width
b) The ratio of PMOS to NMOS sizing
c) Supply voltage
d) Load capacitance

1-e. Which logic gate combination is used in an AOI (AND-OR-Invert) gate? (CO3,K2) 1
a) AND followed by OR
b) OR followed by AND
c) AND followed by NOR
d) OR followed by NAND

1-f. A full adder circuit can be implemented by combining: (CO3,K5) 1
a) Two half adders and an OR gate
b) Two half adders and an AND gate
c) One half adder and a NOT gate
d) Three half adders

1-g. What is the primary issue caused by charge sharing in dynamic logic circuits? (CO4,K2) 1
a) Increased power consumption
b) Logic level degradation leading to incorrect outputs
c) Faster switching speeds
d) Improved noise margins

1-h. In dynamic CMOS logic, during the precharge phase, the output node is: (CO4,K2) 1
a) Discharged to ground
b) Left floating
c) Charged to VDD
d) Connected to the input signal

1-i. In the ASIC backend design flow, which step follows floor planning? (CO5,K2) 1
a) Verification
b) Placement
c) Testing
d) Synthesis

1-j. Which flash memory type is suitable for high-speed random access? (CO5,K2) 1
a) EEPROM
b) NOR Flash
c) NAND Flash
d) DRAM

2. Attempt all parts:-

2.a. Define latch-up in CMOS technology. (CO1,K2) 2

2.b. What is CMOS inverter, draw its truth table? (CO2,K2) 2

2.c. Differentiate between a latch and a flip-flop. (CO3,K2) 2

2.d. Define Domino logic in CMOS circuits. (CO4,K2) 2

2.e. What is the main function of a refresh operation in DRAM? (CO5,K2) 2

SECTION – B 30

3. Answer any <u>five</u> of the following-

3-a. Explain the major steps in CMOS fabrication? (CO1,K2) 6

3-b. What is Gradual channel approximation? Derive the basic current equations for MOS device design. (CO1,K5) 6

3-c. What is the significance of device sizing in CMOS inverter design? (CO2,K2) 6

3-d. Explain the concept of noise margins in CMOS inverters and how they are calculated. (CO2,K2) 6

3-e.	Explain the five regions of operation of a CMOS inverter with the help of VTC curve. (CO3,K2)	6
3-f.	Describe the charge sharing problem in dynamic logic circuits and its impact. (CO4,K2)	6
3-g.	What is flash memory? Write its applications and advantages. (CO5,K2)	6

SECTION – C 50

4. Answer any <u>one</u> of the following-

4-a.	Describe the VLSI design flow in detail with a diagram. (CO1,K2)	10
4-b.	Discuss short channel effects in MOSFETs and their impact on device performance. (CO1,K2)	10

5. Answer any <u>one</u> of the following-

5-a.	Discuss the types of power dissipation in a CMOS inverter and strategies to minimize them. (CO2,K2)	10
5-b.	Consider a CMOS inverter circuit with the following parameters: V DD =3 .3V, V Tn =0.6 V, V TP = -0.7 V, kn= 200 uA/V^2, kp = 80 uA/V^2. Calculate the noise margins of the circuit. (CO2,K5)	10

6. Answer any <u>one</u> of the following-

6-a.	Design a CMOS circuit for a 2-to-1 multiplexer and explain its operation. Draw it using Transmission gate. (CO3,K2)	10
6-b.	Explain the concept of sequential logic circuits and how they differ from combinational logic circuits. Draw NAND, XOR and NOR gates using Pass transistor logic(PTL). (CO3,K2)	10

7. Answer any <u>one</u> of the following-

7-a.	Discuss the operation of a dynamic CMOS logic gate, explaining the precharge and evaluation phases. (CO4,K2)	10
7-b.	Design a dynamic CMOS logic circuit for a 4-input NAND gate and explain its operation. (CO4,K2)	10

8. Answer any <u>one</u> of the following-

8-a.	Discuss the backend VLSI design flow. Highlight the importance of design rule checking (DRC) and layout rules. (CO5,K2)	10
8-b.	Describe the operation and internal architecture of an SRAM cell. Discuss leakage mechanisms. (CO5,K2)	10